Amendments to the Specification:

Please replace paragraph [0075] with the following replacement paragraph:

[0075] The single write of oscillator control register 25 also writes a digital zero to bit four 47, thereby deasserting PriFailEn. Deasserting PriFailEn prevents clock edge detection logic 53 of the primary clock source fail detect block 37 from switching, even if RstPriFailIRQ is not asserted and LFSR 54 is allowed to continue to timeout. Preventing clock edge detection logic 53 from switching reduces power consumption. It is therefore seen that power consumption is reduced in the entire ~~processor~~process of switching from the failed clock source PriClk to the powered up SecClk by: 1) holding LFSR 54 in a reset state, 2) disabling clock edge detection logic 53 from switching, and 3) preventing the output of unecessary interrupts to processor 15 that would otherwise be caused due to the repeated detection of the failed PriClk.